REMARKS

I. General

Claims 1-44 were pending in the present application. The current Office Action (mailed March 7, 2007) rejects claims 1-7, 13, 14, 16-31, and 33-44. Applicant notes with appreciation the indication of claims 8-12, 15, and 32 as being allowable if rewritten in independent form. The outstanding issues raised in the current Office Action are:

- Claims 1-4, 13-14, 16-17, 20-26, 33-34, 36-38 and 40-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,516 issued to Rostoker et al. (hereinafter "*Rostoker*") in view of U.S. Patent No. 7,079,386 issued to Jochym et al. (hereinafter "*Jochym*") and further in view of U.S. Patent Application Publication No. 2003/0088800 to Cai (hereinafter "*Cai*") and still further in view of what the Examiner alleges to be "old and well known in the art", *see* Page 2 of Office Action.

- Claims 5-7, 18-19, 27-31, 35, and 39 are rejected on the ground of nonstatutory obviousness-type double-patenting as being unpatentable over claims 1-9 of U.S. Patent No. 7,072,185 to Belady et al, (hereinafter "*Belady*") in view of *Rostoker* in view of *Jochym* and further in view of *Cai* and further in view of U.S. Patent No. 5,805,915 to Wilkinson et al. (hereinafter "*Wilkinson*") and still further in view of what the Examiner alleges to be "old and well known in the art", *see* Page 4 of Office Action.

Applicant respectfully traverses the outstanding claim rejections raised in the current Office Action, and requests reconsideration and withdrawal thereof in light of the remarks presented herein.

II. Rejections Under 35 U.S.C. §103

Claims 1-4, 13-14, 16-17, 20-26, 33-34, 36-38 and 40-44 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Rostoker* in view of *Jochym* and further in view of *Cai* and still further in view of what the Examiner alleges to be "old and well known in the art" (hereinafter "*Official Notice*"), *see* Page 2 of Office Action. Applicant respectfully traverses these rejections below.

The test for non-obvious subject matter is whether the differences between the subject matter and the prior art are such that the claimed subject matter as a whole would have been obvious to a person having ordinary skill in the art to which the subject matter pertains. The United States Supreme Court in Graham v. John Deere and Co., 383 U.S. 1 (1966) set forth the factual inquiries which must be considered in applying the statutory test: (1) determining of the scope and content of the prior art; (2) ascertaining the differences between the prior art and the claims at issue; and (3) resolving the level of ordinary skill in the pertinent art. As discussed further hereafter, Applicant respectfully asserts that the claims include non-obvious differences over the cited art.

Prima Facie Case Not Established

As an initial matter, Applicant respectfully notes that the Examiner has failed to satisfy the requirements of Graham v. John Deere and Co., 383 U.S. 1 (1966) in the present Office Action. M.P.E.P. §706.02(j) explains that to make out a proper rejection under 35 U.S.C. §103, "the examiner should set forth in the Office action:

(A) the relevant teachings of the prior art relied upon, preferably with reference to the relevant column or page number(s) and line number(s) where appropriate,

(B) the difference or differences in the claim over the applied reference(s),

(C) the proposed modification of the applied reference(s) necessary to arrive at the claimed subject matter, and

(D) an explanation of why one of ordinary skill in the art at the time the invention was made would have been motivated to make the proposed modification."

The present Office action fails to provide at least items B-D identified above. For instance, while the Examiner asserts on page 2 of the Office Action that claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Rostoker* in view of *Jochym* and further in view of *Cai* and still further in view of *Official Notice*, the Examiner fails to identify any difference between claim 1 and the *Rostoker* reference, any proposed modification to the *Rostoker* reference, as well as any explanation as to why one would have been motivated to make such proposed modification (indeed, the Office Action fails to explain any reasoning whatsoever as to why one of ordinary skill in the art would have combined the references). Indeed, the Examiner fails to explain any reliance whatsoever on *Jochym*, *Cai*, and the

Official Notice as applied to claim 1. That is, it appears that the Examiner does not apply *Jochym*, *Cai*, or the *Official Notice* with regard to claim 1, but instead appears to rely solely on *Rostoker* in rejecting claim 1.

In explaining the rejection on page 3 of the Office Action, the Examiner appears to rely upon *Jochym* solely as disclosing "the use of a fourth level shared cache in a multiprocessor system". Irrespective of whether this assertion is accurate, claim 1 does not recite such a fourth level shared cache, and thus *Jochym* does not appear to be relied upon in rejecting claim 1.

The Examiner appears to rely upon *Cai* solely as disclosing "a multiprocessor system that comprises a method for regulating the power consumption of the system by adjusting the operating frequencies of the processors while maintaining an overall level of system performance", *see* page 3 of the Office Action. Irrespective of whether this assertion is accurate, claim 1 does not recite such a method for regulating the power consumption by adjusting operating frequencies of the processors, and thus *Cai* does not appear to be relied upon in rejecting claim 1.

The Examiner appears to rely upon *Official Notice* solely for the assertion that "Intel Itanium processors are well known", "to include multiple processor modules in a computer system" is well known, and "power cabling" is well known, *see* page 3 of the Office Action. Irrespective of whether these assertions are accurate, claim 1 does not recite such features, and thus *Official Notice* does not appear to be relied upon in rejecting claim 1.

The rejection of claims 1-4, 13-14, 16-17, 20-26, 33-34, 36-38 and 40-44 is treated fully on page 3 of the Office Action, and as evidenced by the above discussion of claim 1, the Office Action fails to identify/explain to what extent, if at all, each reference is relied upon in rejecting each claim. For instance, while claim 1 stands rejected as unpatentable over *Rostoker* in view of *Jochym* and further in view of *Cai* and still further in view of *Official Notice*, *see* page 2 of the Office Action, the Office Action fails to explain any reliance whatsoever on *Jochym*, *Cai*, and *Official Notice* in rejecting claim 1.

Accordingly, the current rejection is improper for at least the above reasons, and thus in the event that the current claims are not found allowable by the Examiner after

consideration of the remarks presented herein, a proper rejection that complies with the above-noted requirements of Graham v. John Deere and Co., 383 U.S. 1 (1966) and M.P.E.P. §706.02(j) should be presented in a non-final Office Action to afford Applicant a full and fair opportunity to respond thereto.

Independent Claim 1

Independent claim 1 recites:

> An apparatus comprising:
> a plurality of logically independent processors;
> a system bus; and
> a cache control and bus bridge device in communication with the plurality of processors such that it is logically interposed between the processors and the system bus, and wherein the processors and cache control and bus bridge device are disposed in a module form factor such that the apparatus is a drop-in replacement for a standard single-processor module. (Emphasis added).

The combination of *Rostoker*, *Jochym*, *Cai*, and *Official Notice* fails to disclose at least the above-emphasized element of claim 1. As discussed above, it appears that the Examiner relies solely upon *Rostoker* in rejecting claim 1. However, *Rostoker* fails to disclose at least "wherein the processors and cache control and bus bridge device are disposed in a module form factor such that the apparatus is a drop-in replacement for a standard single-processor module", as recited by claim 1. *Rostoker* appears to be directed to forming a plurality of processors on a single integrated circuit chip together with a memory controller and an I/O controller, *see* Abstract of *Rostoker*. However, *Rostoker* fails to provide any teaching or disclosure whatsoever of disposing such elements in a module form factor such that the apparatus is a drop-in replacement for a standard single-processor module. No such drop-in replacement compatibility with a single-processor module is mentioned whatsoever by *Rostoker*.

Accordingly, because *Rostoker* fails to disclose at least the above-identified element of claim 1, the rejection should be withdrawn.

Independent Claim 16

Independent claim 16 recites:

> A method comprising:
> connecting on a local bus a plurality of processors such that the processors are logically independent;
> logically interposing between the local bus and a system bus an in-line cache control and bus bridge device;
> disposing in a module conforming to a standard single-processor module form factor the plurality of processors, the local bus, and the in-line cache control and bus bridge device; and
> operating the plurality of processors and the in-line cache control and bus bridge device such that data input to each of the processors is processed independently and simultaneously. (Emphasis added).

The combination of *Rostoker*, *Jochym*, *Cai*, and *Official Notice* fails to disclose at least the above-emphasized element of claim 16. As with claim 1, it appears that the Examiner relies solely upon *Rostoker* in rejecting claim 16, *see* page 3 of the Office Action. However, *Rostoker* fails to disclose at least "disposing in a module conforming to a standard single-processor module form factor the plurality of processors, the local bus, and the in-line cache control and bus bridge device", as recited by claim 16. *Rostoker* appears to be directed to forming a plurality of processors on a single integrated circuit chip together with a memory controller and an I/O controller, *see* Abstract of *Rostoker*. However, *Rostoker* fails to provide any teaching or disclosure whatsoever of disposing such elements in a module conforming to a standard single-processor module form factor. No such conformance of a module to a standard single-processor module form factor is mentioned whatsoever by *Rostoker*.

Accordingly, because *Rostoker* fails to disclose at least the above-identified element of claim 16, the rejection should be withdrawn.

Independent Claim 33

Independent claim 33 recites:

> A multi-processor module comprising:
> a plurality of logically parallel processors;
> a system bus; and
> a cache control and bus bridge device in communication with the plurality of processors such that it is logically interposed between the processors and the system bus, and wherein the processors and cache control and bus bridge device are disposed in a module that is compatible with a single-processor module interface. (Emphasis added).

The combination of *Rostoker*, *Jochym*, *Cai*, and *Official Notice* fails to disclose at least the above-emphasized element of claim 33. As with claim 1, it appears that the Examiner relies solely upon *Rostoker* in rejecting claim 33, *see* page 3 of the Office Action. However, *Rostoker* fails to disclose at least "wherein the processors and cache control and bus bridge device are disposed in a module that is compatible with a single-processor module interface", as recited by claim 33. *Rostoker* appears to be directed to forming a plurality of processors on a single integrated circuit chip together with a memory controller and an I/O controller, *see* Abstract of *Rostoker*. However, *Rostoker* fails to provide any teaching or disclosure whatsoever of disposing such elements in a module that is compatible with a single-processor module interface. No such compatibility of a multi-processor module with a single-processor module interface is mentioned whatsoever by *Rostoker*.

Accordingly, because *Rostoker* fails to disclose at least the above-identified element of claim 33, the rejection should be withdrawn.

Independent Claim 36

Independent claim 36 recites:

> A multi-processor module comprising:
> a plurality of processors;
> a cache control and bus bridge device that controls access to a common cache by the plurality of processors and electrically isolates the processors from a system bus. (Emphasis added).

The combination of *Rostoker*, *Jochym*, *Cai*, and *Official Notice* fails to disclose at least the above-emphasized element of claim 36. As with claim 1, it appears that the Examiner relies solely upon *Rostoker* in rejecting claim 36, *see* page 3 of the Office Action. However, *Rostoker* fails to disclose at least "a cache control and bus bridge device that controls access to a common cache by the plurality of processors and electrically isolates the processors from a system bus", as recited by claim 36. *Rostoker* appears to be directed to forming a plurality of processors on a single integrated circuit chip together with a memory controller and an I/O controller, *see* Abstract of *Rostoker*. The Examiner appears to allege that the memory control/IO control of *Rostoker* provides the recited cache control and bus bridge device. However, *Rostoker* fails to provide any teaching or disclosure whatsoever of such memory control/IO control of *Rostoker* electrically isolating the processors from a system bus, as recited by claim 36. No such electrical isolation of the processors from the system bus appears to be mentioned whatsoever by *Rostoker*.

Accordingly, because *Rostoker* fails to disclose at least the above-identified element of claim 36, the rejection should be withdrawn.

Independent Claim 41

Independent claim 41 recites:

> A system comprising:
> means for connecting a module to a system board through an interface compatible with a standard single-processor module;
> means for interfacing the system board to a computer system platform;
> means for inputting data to the module from the system board via a system bus
> means for processing the data by a plurality of processors such that each processor processes some of the data independently and simultaneously to the other processors of the plurality; and
> means for receiving by components in the system board processed data from the module via the system bus. (Emphasis added).

The combination of *Rostoker*, *Jochym*, *Cai*, and *Official Notice* fails to disclose at least the above-emphasized element of claim 41. As with claim 1, it appears that the Examiner relies solely upon *Rostoker* in rejecting claim 41, *see* page 3 of the Office Action. However, *Rostoker* fails to disclose at least "means for connecting a module to a system board through an interface compatible with a standard single-processor module", wherein data input to the module from the system board is processed by a plurality of processors, as recited by claim 41. *Rostoker* appears to be directed to forming a plurality of processors on a single integrated circuit chip together with a memory controller and an I/O controller, *see* Abstract of *Rostoker*. However, *Rostoker* fails to provide any teaching or disclosure whatsoever of disposing such elements in a module that connects to a system board through an interface that is compatible with a standard single-processor module. No such compatibility of a multi-processor module with a single-processor module interface is mentioned whatsoever by *Rostoker*.

Accordingly, because *Rostoker* fails to disclose at least the above-identified element of claim 41, the rejection should be withdrawn.

Dependent Claims

Claims 2-4, 13-14, 17, 20-26, 34, 37-38, 40, and 42-44 each depend from one of independent claims 1, 16, 33, 36, and 41, and are thus likewise believed to be allowable at least based on their dependency from their respective independent claim for the reasons

discussed above. Accordingly, Applicant respectfully requests that the rejection of claims 2-4, 13-14, 17, 20-26, 34, 37-38, 40, and 42-44 also be withdrawn.

III. The Nonstatutory Obviousness-Type Double Patenting Rejections

Claims 5-7, 18-19, 27-31, 35, and 39 are rejected on the ground of nonstatutory obviousness-type double-patenting as being unpatentable over claims 1-9 of *Belady* in view of *Rostoker* in view of *Jochym* and further in view of *Cai* and further in view of *Wilkinson* and still further in view of what the Examiner alleges to be "old and well known in the art" (hereinafter "*Official Notice*"), *see* Page 4 of Office Action.. Applicant respectfully traverses for the reasons stated below.

An obviousness-type double patenting rejection should make clear the differences between the inventions defined by the conflicting claims—a claim in the patent compared to a claim in the application, and the reasons why a person of ordinary skill in the art would conclude that the invention defined in the claim at issue would have been an obvious variation of the invention defined in a claim in the patent. M.P.E.P. § 804(II)(B)(1).

Further, *Belady* is a patent having a filing date later than the filing date of the present application, and thus two-way obviousness must be established, *see* M.P.E.P. § 804(II)(B)(1)(b). Accordingly, to establish a proper grounds of obviousness-type double patenting, the Examiner must apply the *Graham* obviousness analysis twice, once with the present application's claims as the claims in issue and once with *Belady's* claims as the claims in issue. *Id.* The present Office Action fails to do so, and thus fails to properly establish grounds for the obviousness-type double patenting rejection.

Claim 1 of *Belady* recites, in part, "a system board with pass-thru holes" and "wherein the thermal dissipation device extends through at least one of the pass-thru holes". No reasoning whatsoever has been identified regarding why this element of claim 1 of *Belady* would be obvious from the claims of the present application. As noted above, two-way obviousness is required to be established to support the outstanding double-patenting rejection.

Further, as discussed above, *Rostoker* fails to disclose a multi-processor module that is compatible with an interface for a single-processor module. Further, the claims of *Belady* fail to recite such feature. Thus, the Examiner has failed to establish obviousness as for any of the claims of the present application that recite this feature.

Accordingly, Applicant respectfully requests that the Examiner withdraw the obviousness-type double patenting rejection of record. Alternatively, Applicant requests that the Examiner follow the requirements of M.P.E.P. § 804(II)(B)(1) in a subsequent, non-final Office Action, so that Applicant is afforded a full and fair opportunity to respond.

IV. Conclusion

In view of the above, Applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 08-2025, under Order No. 200309347-2 from which the undersigned is authorized to draw.

Respectfully submitted,

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with § 1.6(a)(4).

Dated: May 25, 2007 Signature: Donna Forbit
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